34. The method of claim 13, wherein said depositing said metal containing silicon or said metal alloy is for extending a temperature window in which a silicide metal-rich phase exists.

35. The method of claim 25, wherein said first forming silicide phase comprises a silicon-rich phase.

C6 cont.

36. The method of claim 25, wherein said depositing said metal containing silicon or said metal alloy is for extending a temperature window in which a silicide metal-rich phase exists.

37. The method of claim 26, wherein said first silicide phase comprises a silicon-rich phase.

38. The method of claim 26, wherein said depositing said metal containing silicon or said metal alloy is for extending a temperature window in which a silicide metal-rich phase exists.--

REMARKS

It is noted that a Supplemental Amendment was filed on June 5, 2002, via facsimile. However, such was not referenced in the October 1, 2002, Office Action, and thus a telephone call was placed to the above-identified Examiner to confirm entry of the same. If the Supplemental Amendment has not yet been entered, Applicant respectfully requests entry prior to entry of this Amendment.

Claims 1-8, 10-13, and 23-38 are all the claims presently being examined in the application. New claims 27-38 have been added to more completely define the invention.

Claims 1-8, 10-13, and 23-26 stand rejected on prior art grounds. Claims 1-8, 10-13, and 26 stand rejected upon informalities (e.g., 35 U.S.C. § 112, second paragraph).

With respect to the prior art rejections, claim 25 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Besser, et al. (U.S. Patent No. 6,165,903). Claim 25 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Kanamori, et al. (U.S. Patent Application No. 2002/0009856). Claims 1-2, 4-5, 8, 10, 12-13, 23-24, and 26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Besser, et al., in view of Cabral, Jr., et al. (U.S. Patent No. 5,828,131). Claims 10 and 11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Besser, et al., in view of Akram (U.S. Patent Application No. 2002/0106879). Claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Besser, et al., in view of Akram and Kanamori, et al. Claims 1, 3, 13, and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kanamori, et al., in view of Cabral, Jr., et al. Claims 2, 4-5, 7-8, and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kanamori, et al., in view of Cabral, Jr., et al., as applied to claim 1, and further in view of Besser, et al.

These rejections are respectfully traversed in view of the following discussion.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment.

It is noted that the claim amendments herein are made only for more particularly pointing

out the invention for the Examiner, and not for distinguishing the invention over the prior art, narrowing the claims, or for any statutory requirements of patentability.

Further, it is noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

I. THE CLAIMED INVENTION

Applicant's invention, as disclosed and claimed (e.g., see independent claim 1), is directed to a method for fabricating a silicide for a semiconductor device, which includes depositing a metal containing silicon or a metal alloy on a silicon substrate, reacting the metal containing silicon or the metal alloy to form a first silicide phase, etching any unreacted metal containing silicon, depositing a silicon cap layer over the first silicide phase, reacting the silicon cap layer to form a second silicide phase, for the semiconductor device, and etching any unreacted silicon from the silicon cap layer.

Independent claims 4, 10, 13, 25, and 26 recite somewhat similar methods, but with some different limitations.

With such features, a reaction of metal (e.g., Co in an exemplary embodiment, but other metals will be similarly operable as claimed and as clearly described in the specification) to initially form Co_2Si, minimizes the silicon consumption of the thin SOI film (or bulk silicon) substrate. The consumption of the thin SOI film is additionally reduced by the deposition of a

silicon (or poly-silicon in a non-limiting exemplary variation of the invention) film on the Co_2Si.

With the present invention, the use of a salicide-like process is extended to thin SOI films, which are expected to be used in future SOI MOSFETs. Such thin-film SOI films will be advantageous in making the devices smaller, thereby reducing the source/drain to substrate overlap capacitance, and eliminating the floating body voltage.

Moreover, good control is obtained in forming a silicide over the source and drain in bulk crystalline silicon structures as well as thin film SOI structures.

Such features are not taught or suggested by any other prior art of record, either alone or in combination.

II. THE 35 U.S.C. §112, SECOND PARAGRAPH, REJECTION

While Applicant submits that the claims are clear to one of ordinary skill in the art to recognize the metes and bounds of the invention, to speed prosecution, Applicant notes that claims 1-8, 10-13, and 26 have been amended in a manner believed fully responsive to the Examiner's criticisms.

It is noted that the "alloy" defined by the independent claims is a "metal alloy" which may, or may not, include only metals. That is, the metal alloy could include a metal and another metallic material or it could include a metal and a non-metallic material(s) such as a semiconductor material. Thus, to clarify the Examiner's query on page 3 of the Office Action,

semiconductor material. Thus, to clarify the Examiner's query on page 3 of the Office Action, the metal alloy of the independent claims may include silicon, but there is no requirement in the independent claims that the "metal alloy" includes silicon.

With regard to claim 5, the Examiner's criticism is not completely understood. That is, as described in the application, blanket deposition can be performed from multiple targets (e.g., including first and second materials such as cosputtering with a metal target and a silicon target or the like) or sputtering with a single target comprising an alloy of metal and, for example, a semiconductor material. Blanket deposition means that the "same thing" is deposited over the layer, as opposed to selective deposition in which the material is deposited on selected locations of an underlying layer.

Further, it is noted that claim 5 requires "*wherein said depositing of said metal containing silicon comprises performing a blanket deposition of a metal comprising one of Co and Ti.*" Such language uses the open-ended "comprising" transitional phrase. Thus, in claim 5, the depositing step includes the blanket deposition of a metal comprising either cobalt or titanium. Such language does not preclude or render inconsistent the requirement of claim 4 that a metal (e.g., cobalt or titanium) containing silicon be deposited or that the metal alloy (e.g., cobalt and another material, or titanium and another material) be deposited.

In view of the foregoing, reconsideration and withdrawal of this rejection are respectfully requested.

III. THE PRIOR ART REJECTIONS

A. The §102(e) Rejections of Claim 25 Based on Besser et al. or Kanamori

First, it is noted that the Examiner clearly admits (e.g., see Items No. 9, 10, 12, etc.) that Besser et al. and Kanamori each fails to teach or suggest "*a metal alloy or metal alloy containing silicon was deposited to form the silicide*". Claim 25 clearly requires a "metal containing silicon or a metal alloy...". Thus, on its face, the Examiner's rejection is flawed.

More specifically, Besser et al. discloses a method of forming ultra-shallow junctions in a semiconductor wafer with deposited silicon layer to reduce silicon consumption during salicidation.

Further, Kanamori discloses a method of fabricating a semiconductor device self-aligned silicide areas formed using a supplemental silicon overlayer. Such methods are completely and fundamentally different from that of the invention defined by independent claim 25.

Specifically, the claimed invention defined by claim 25 is clearly distinguished from Besser and Kanamori by the use of a metal alloy or a metal containing silicon (e.g., Co_xSi_{1-x}; a metal-silicon mixture), rather than a pure metal. The use of the alloy encapsulates two important advantages of the claimed invention, which are not shared by Besser and/or Kanamori.

First, the metal-silicon mixture already contains some of the silicon required to form the silicide. Thus, less silicon is consumed from the substrate during the subsequent anneal. Indeed,

none of the references teaches or suggests using such a metal-silicon mixture, let alone for the reason and purpose of the invention.

Secondly, as clearly defined by claim 25, a metal alloy may be deposited instead of the metal-silicon mixture. As mentioned above, the "metal alloy" means a metal and another material (e.g., another metal, a semiconductor, etc.). Using such a metal alloy enables applying the silicon cap to the very first forming phase (e.g., Co_2Si), rather than a later phase (e.g., CoSi) as allegedly taught by Besser and Kanamori.

Indeed, the known metal (e.g., cobalt will be employed in this exemplary embodiment) silicide phases in the order that they form are illustrated in Figure 1 of Exhibit I which was attached to the Amendment filed on May 14, 2002, and for convenience the Examiner is referred thereto. The resistivity and formation temperature of each phase are also indicated. By applying the silicon cap to the Co_2Si phase, silicon is supplied from the cap already during the reaction that forms the CoSi phase. The silicon consumption from the substrate is then reduced during the formation of the CoSi and the $CoSi_2$ phase, which is a significant improvement over the methods of Besser and/or Kanamori.

Furthermore, as noted in the previous Amendment, the use of the metal-silicon mixture is fundamental to the inventive method and is neither anticipated nor rendered obvious by Besser and/or Kanamori. Indeed, referring to the diffraction maps shown in Figures 2A and 2B of Exhibit I submitted with the Amendment on May 14, 2002, the top map (e.g., Figure 2A) shows the evolution of the Co-silicide phases when pure Co metal is used (as opposed to a metal

containing silicon or an alloy, as in the claimed invention).

At a temperature lower than about 440 °C, no reaction takes place, and only pure Co is measured. Then, when the temperature is increased, the Co_2Si phase forms and exists only within a narrow window of about 20 °C, after which the phase changes into CoSi.

The CoSi phase persists up to 625 °C where it changes into $CoSi_2$. Since the Co_2Si phase only exists in a very narrow, tight temperature window, it is very difficult to form (e.g., very unreliable and prone to error or being missed based on nonuniform doping of the substrate, etc.), and, in practice, the later phase (e.g., CoSi) is used in self-aligned silicide processes.

The bottom map (e.g., Figure 2B) shows the evolution of reacting a metal (e.g., Co) containing silicon or a metal alloy, as in the claimed invention.

That is, Figure 2B shows the metal (e.g., Co)-silicide phases when a Co-silicon mixture having 20% silicon is used instead of pure Co. In this case, the Co_2Si phase exists over a large temperature window of more than 100 °C. This makes it possible to practice a self-aligned silicide process where the first phase is also the first forming phase (Co_2Si). As a result, much more reliable and easier manufacturing processes are possible since it is easier to stop on Co_2Si, etc. Then, annealing can be performed, etc. to go to CoSi, and finally to $CoSi_2$.

Again, Applicant submits that such is not trivial to use the method above (including using the metal-silicon mixture or a metal alloy), and thus, it is clear that neither Besser nor Kanamori anticipate or render obvious claim 25 of the present application.

Thus, using the metal containing silicon or a metal alloy, as in the invention, produces

unexpectedly superior results, as clearly shown in a comparison of the Figures in Exhibit 1. Again, in the invention, including some of the silicon in the metal is better than what Besser is doing since less silicon is consumed in the inventive method. That is, some of the silicon is being provided by the metal-silicon mixture or alloy.

Further (and maybe more importantly), using the metal-silicon mixture (or metal alloy) does not simply allow more silicon to be provided, but it allows the invention to stop on the first silicide forming phase (e.g., Co_2Si) because a wider temperature window is being provided. Again, the inventors have recognized that providing the silicon cap as early as possible in the process, is advantageous.

That is, if the silicon cap is provided when the phase is, for example, Co_2Si, then another source of silicon is provided, thereby reducing (e.g., halving) the amount of silicon needed from the substrate or the like in the next phase (e.g., CoSi).

Besser, at most, starts to obtain the benefit of applying the silicon cap (if any) only at the very last phase (e.g., forming of the $CoSi_2$ phase), not the very first forming silicide phase as in claim 25. Again, the invention applies the cap much earlier, and hence, the invention obtains the benefit of the cap much earlier.

In sum, the invention applies and reacts the metal containing silicon or a metal alloy to form a first silicide phase. Indeed, Besser and Kanamori do not even address the forming of phases.

Further, there is no teaching or suggesting of reacting a metal containing silicon or a

metal alloy to form the first forming silicide phase, as defined by independent claim 25.

That is, the invention wants to react the metal containing silicon or metal alloy in the phase which is first formed. The inventors have recognized that, as the reaction continues, more and more silicon is consumed. Thus, the invention recognizes that performing the reacting to form the phase which consumes as little silicon as possible is the most desirable. Hence, the invention of independent claim 25 reacts the metal containing silicon or the metal alloy in the very first phase which is formed. However, none of the references has even recognized the advantages of even performing such an operation.

Moreover, both Besser and Kanamori are mute about the lowest consumption phase, Co_2Si, and only discuss the high resistivity phase CoSi as the first silicide phase to be used in their processes. CoSi is not the first forming phase and thus is clearly distinguished from the claimed invention.

Turning to the clear language of independent claim 25, there is no teaching or suggestion of "*[a] method for fabricating a silicide for a semiconductor device, said method comprising:*

depositing a metal containing silicon or a metal alloy on a silicon substrate;

reacting said metal containing silicon or said metal alloy to form a first forming silicide phase;

etching any unreacted metal or alloy;

depositing a silicon cap layer over said first forming silicide phase;

reacting the silicon cap layer to form a second silicide phase, for said semiconductor

device; and

etching any unreacted silicon from said silicon cap layer (emphasis Applicant's).

Hence, the invention defined by independent claim 25 is not anticipated nor rendered obvious by any of Besser and Kanamori.

B. The §103 Rejection based on Besser et al. in view of Cabral (5,828,131)

Regarding the §103 rejection of claims 1-2, 4-5, 8, 10, 12-13, 23-24 and 26, Besser and its deficiencies have been discussed above. The Examiner refers to column 6, lines 4-16 and to column 11, lines 4-11 of Cabral in urging that Cabral makes up for the deficiencies of Besser. However, this is erroneous, and clearly Cabral fails to make up for the deficiencies of Besser.

That is, the $TiSi_2$ phase can exist in two polycrystalline structures. The first polycrystalline structure, known as the "C49 phase", has a resistivity of about 60-90 micro-ohm-cm. The second polycrystalline structure, known as the "C54 phase", has a lower resistivity of about 12-20 micro-ohm-cm, and is therefore the desired phase. The C49 phase forms at about 650 °C. The C54 phase forms at a higher temperature of about 766 °C (See Fig 12 in Cabral). The high formation temperature can lead to device degradation, and agglomeration of the silicide film if a high enough anneal temperature is used to ensure the phase transformation for small circuit features. Cabral et al. is addressing the issue of the high temperature anneal required to form the low resistivity C54 phase, and proposes a method for lowering the formation

form the low resistivity C54 phase, and proposes a method for lowering the formation temperature. It is noted that this issue is rather specific to titanium silicide and does not apply to all silicides in general.

Cabral proposes depositing a Ti film over a refractory metal such as Ta, Nb, Mo, or W, and annealing to form a C54 $TiSi_2$ phase. In a different embodiment, Cabral deposits a Ti-Si alloy over the refractory metal. This alloy is targeted to be stoichiometric $TiSi_2$, but may be richer or leaner in its silicon composition (See column 6, lines 4-17).

First, Applicant submits that, given the disparate problems faced by each of Besser, Cabral and the present invention, it would not have made it "obvious" to combine the references, absent impermissible hindsight construction of the present invention, made possible only through a keyword search by the Examiner after a thorough reading of Applicant's own specification. Indeed, Cabral is trying to solve a different problem than that addressed by the present invention, as explained below.

Secondly, Cabral is not proposing a process which reduces silicon consumption. Cabral's proposes a method for forming the C54-$TiSi_2$ at a lower temperature than the conventional method, and preferably with one anneal.

Cabral (similarly to Besser) is silent with respect to forming any of the intermediate silicon-rich phases. When annealing Ti over silicon, the following phases form with increased temperature:

Ti -> Ti_3Si -> Ti_5Si_3 -> Ti_5Si_4 -> TiSi -> C49-$TiSi_2$ -> C54-$TiSi_2$.

In contrast to Cabral, following the method of the present invention, one would first form a silicon-rich phase, such as the Ti_5Si_3 phase, etch the unreacted Ti, apply a silicon cap, and then run a second anneal to form the C54-$TiSi_2$ phase.

Cabral does not teach or suggest forming the Ti_5Si_3 phase or any other intermediate phase, but actually proposes a method that forms the final phase C54-$TiSi_2$ in one annealing step. Indeed, Cabral attempts to avoid the second "conversion-anneal". His process will preferably have one anneal step that will form the C54 $TiSi_2$ phase (See for example, column 2, lines 23-30, and column 6, lines 22-26).

Additionally, the embodiment in which Cabral proposes using a near stoichiometric $TiSi_2$ alloy, cannot be applied to the self-aligned silicide (SALICIDE) method. The SALICIDE process includes applying a blanket metal film (such as Ti) onto a device structure (such as a MOSFET), annealing the wafer to react the metal with silicon surfaces to form a silicide (the metal over insulator surfaces, such as the MOSFET's sidewalls, does not convert into a silicide and remains a metal), etching the unreacted metal, and performing a second anneal to reach the desired silicide phase. The etching of the unreacted metal is essential to prevent bridging which otherwise will short the device source or drain area to the gate.

The above-described process is summarized in Cabral on column 1, line 47-55, and on column 11, line 48 to column 12, line 18. The etching is selective in the sense that it attacks the pure metal, but does not attack the silicide.

The SALICIDE process cannot be performed with a blanket deposited Ti - Silicon alloy

(as opposed to Ti alloy, which is defined in Cabral as Ti with some refractory metal) having a composition of stoichiometric $TiSi_2$, since the selective etch would no longer work. When a pure Ti or metallic Ti alloy is used, the metal over the device spacers does not convert into silicide during the anneal. Therefore, the unreacted metal can be etched since the etchant attacks only the metal, and does not remove silicide.

In contrast, when a near stoichiometric Ti-Silicon alloy is blanket deposited, the spacers are covered with a Ti silicide the same as the rest of the device surfaces and the selectivity of metal versus silicide is lost. It is noted that this is precisely one of the reasons that Cabral specifies the refractive metal for forming the Ti alloy as being "preferably a metal that is capable of forming a metal silicide" (column 3, lines 65-66). In addition, Cabral describes the application of his invention to the SALICIDE method only with Ti alloy (column 11, lines 48-65).

Cabral is "skipping" the intermediate silicide phases. In contrast, Applicants are using a metal-silicon alloy to extend the temperature window in which the silicide metal-rich phase exists.

For example, this temperature window is extended from 20 °C to over 100 °C in the case of Co_2Si. This allows the invention to reliably form the metal-rich phase and apply the silicon cap as early as possible in the SALICIDE process. In complete and fundamental contrast, Cabral is trying to minimize the temperature window where the metal-rich silicide exists so that the final phase (C54-$TiSi_2$) will form at a lower temperature than that of the conventional method.

Thus, Applicants submit that Besser and Cabral would not have been combined by one of

ordinary skill in the art at the time of the invention and absent hindsight.

Additionally, even assuming arguendo that Besser and Cabral would have been combined in the manner urged, the claimed invention would still not have been produced. Thus, claims 1, 2, 4, 5, 8, 10, 12, 13, 23, 24, and 26 are patentable over the Examiner's proposed combination.

C. The §103 Rejection based on Besser et al. in view of Akram (US 2002/0106879)

Regarding the §103 rejection of claims 10 and 11, Besser and its deficiencies (e.g., lack of teaching a metal alloy or a metal alloy containing silicon being deposited to form a silicide) have been discussed above. The Examiner refers to paragraphs 34 and 39 of Akram in urging that Akram makes up for the deficiencies of Besser. However, this is erroneous, and clearly Akram fails to make up for the deficiencies of Besser.

Akram addresses the issue of stress notches (also known as "stress voids") in interconnect lines. While Akram's main focus is on pure metals for conductive lines due to their high conductance, he also suggests using "a metal alloy or a metal compound" (paragraph [34]). Examples of the latter are titanium nitride, TiW, and titanium silicide.

However, one of ordinary skill in the art would not have been motivated to combine the teachings of Akram with those of Besser, absent hindsight.

Specifically, Akram's invention is not related to the SALICIDE method, nor is it applicable to forming a silicide for a MOSFET device. Additionally, the structures proposed by

Akram are built on insulator layers where there is not any silicon. Thus, the issue of silicon consumption is immaterial and is irrelevant to the Examiner's urged combination.

Additionally, as to the Examiner comment No. 10 on page 6 of the Office Action in which the Examiner asserts that "Akram teaches a method of forming silicides by depositing metal and metal alloys including silicides...", this is not the case.

That is, Akram merely teaches that a metal, or a metal alloy, or even a silicide can be used as the conductor material in Akram's structure (e..g., layer 8 in paragraph [034]). It is noted that in paragraph [035] Akram is reviewing what is common knowledge as to how a silicide is formed: "*[i]f metal layer 8 is a metal silicide, it may be formed, for example, by first depositing either a metal layer or a silicon layer, then depositing the other, and heating to react the two layers and form a silicide*". There is no other silicide teaching in Akram's application.

Thus, there would have been no motivation to combine Akram with Besser, and even if the Examiner's urged combination would have been made the claimed invention would still not have resulted. Thus, claims 10 and 11 are patentable over the Examiner's urged combination of Besser in view of Akram.

Additionally, regarding the rejection of claim 6, based on Besser, Akram and Kanamori, Kanamori would not have been combined with the references for the same reasons discussed above. Further, Kanamori fails to make up for the deficiencies of Besser and Akram discussed above. Thus, claim 6 is similarly patentable.

D. The §103 Rejection based on Kanamori in view of Cabral

Regarding the §103 rejection of claims 1, 3, 13, and 23, Kanamori and its deficiencies have been discussed above. The Examiner admits that Kanamori fails to teach or suggest a metal alloy or metal alloy containing silicon deposited to form a silicide, but again refers to column 6, lines 4-16 and to column 11, lines 4-11 in urging that Cabral makes up for the deficiencies of Kanamori. However, this is erroneous, and clearly Cabral fails to make up for the deficiencies of Kanamori for all of the reasons discussed above.

Specifically and for the record, the $TiSi_2$ phase can exist in two polycrystalline structures.

The first polycrystalline structure (e.g., the C49 phase) has a resistivity of about 60-90 micro-ohm-cm. The second polycrystalline structure (e.g., the C54 phase) has a lower resistivity of about 12-20 micro-ohm-cm, and is therefore the desired phase. The C49 phase forms at about 650 °C. The C54 phase forms at a higher temperature of about 766 °C (See Fig 12 in Cabral). Such a high formation temperature can lead to device degradation, and agglomeration of the silicide film if a high enough anneal temperature is used to ensure the phase transformation for small circuit features. Cabral et al. is addressing the issue of the high temperature anneal required to form the low resistivity C54 phase, and proposes a method for lowering the formation temperature. Again, it is noted that this issue is rather specific to titanium silicide and does not apply to all silicides in general.

Cabral proposes depositing a Ti film over a refractory metal such as Ta, Nb, Mo, or W,

and annealing to form a C54 $TiSi_2$ phase. In a different embodiment, Cabral deposits a Ti-Si alloy over the refractory metal. This alloy is targeted to be stoichiometric $TiSi_2$, but may be richer or leaner in its silicon composition (See column 6, lines 4-17).

Cabral is trying to solve a different problem than that addressed by the present invention as explained above and as reiterated below. Hence, Applicant submits that, given the very different problems faced by each of Kanamori, Cabral and the present invention, as well as the very different solutions each provides to such different problems, it would not have been "obvious" to combine the references, absent impermissible hindsight construction of the present invention.

First, Cabral is not proposing a process which reduces silicon consumption. Indeed, Cabral does not even recognize that such would be useful. Cabral's proposes a method for forming the C54-$TiSi_2$ at a lower temperature than the conventional method, and preferably with only one anneal.

Cabral (similarly to Besser) is silent with respect to forming any of the intermediate silicon-rich phases. When annealing Ti over silicon, the following phases form with increased temperature:

Ti -> Ti_3Si -> Ti_5Si_3 -> Ti_5Si_4 -> TiSi -> C49-$TiSi_2$ -> C54-$TiSi_2$.

Following the method of the present invention, one would first form a silicon-rich phase, such as the Ti_5Si_3 phase, etch the unreacted Ti, apply a silicon cap, and then perform a second

anneal to form the C54-$TiSi_2$ phase. Cabral does not teach or suggest forming the Ti_5Si_3 phase or any other intermediate phase, but actually proposes a method that forms the final phase C54-$TiSi_2$ in one annealing step. As mentioned above, Cabral attempts to avoid the second "conversion-anneal". Cabral's process will preferably have one anneal step that will form the C54 $TiSi_2$ phase (See for example, column 2, lines 23-30, and column 6, lines 22-26).

Additionally, the embodiment in which Cabral proposes using a near stoichiometric $TiSi_2$ alloy, cannot be applied to the self-aligned silicide (SALICIDE) method, as explained above.

That is, the SALICIDE process includes applying a blanket metal film (such as Ti) onto a device structure (such as a MOSFET), annealing the wafer to react the metal with silicon surfaces to form a silicide (i.e., the metal-over-insulator surfaces, such as the MOSFET's sidewalls, does not convert into a silicide and remains a metal), etching the unreacted metal, and then performing a second anneal to reach the desired silicide phase. The etching of the unreacted metal is essential to prevent bridging which otherwise will short the device source or drain area to the gate.

The above-described process is summarized in Cabral on column 1, line 47-55, and on column 11, line 48 to column 12, line 18. As mentioned above, the etching is "selective" in that it attacks the pure metal, but does not attack the silicide.

The SALICIDE process cannot be performed with a blanket deposited Ti-Silicon alloy (as opposed to Ti alloy, which is defined in Cabral as Ti with some refractory metal) having a composition of stoichiometric $TiSi_2$, since the selective etch would no longer work. When a pure Ti or metallic Ti alloy is used, the metal over the device spacers does not convert into silicide

during the anneal. Therefore, the unreacted metal can be etched since the etchant attacks only the metal, and does not remove silicide.

In contrast, when a near stoichiometric Ti-Silicon alloy is blanket-deposited, the spacers are covered with a Ti silicide the same as the rest of the device surfaces and the selectivity of metal versus silicide is lost. As noted above, this is why Cabral specifies the refractive metal for forming the Ti alloy as being "preferably a metal that is capable of forming a metal silicide" (column 3, lines 65-66). In addition Cabral describe the application of his invention to the SALICIDE method only with Ti alloy (column 11, lines 48-65).

Cabral "skips" the intermediate silicide phases. As has been discussed above and in previous responses, the present invention uses a metal-silicon alloy to extend the temperature window in which the silicide metal-rich phase exists.

For example, this temperature window is extended from 20 °C to over 100 °C in the case of Co_2Si. This allows the invention to reliably form the metal-rich phase and apply the silicon cap as early as possible in the SALICIDE process. In complete and fundamental contrast, Cabral is trying to minimize the temperature window where the metal-rich silicide exists so that the final phase (C54-$TiSi_2$) will form at a lower temperature than that of the conventional method.

Thus, Applicants submit that Kanamori and Cabral would not have been combined, by one of ordinary skill in the art at the time of the invention and absent hindsight.

Additionally, even assuming arguendo that Kanamori and Cabral would have been combined in the manner urged, the claimed invention would still not have been produced. Thus,

claims 1, 3, 13, and 23 are patentable over the Examiner's proposed combination of Kanamori and Cabral.

Additionally, regarding the rejection of claims 2, 4, 5, 7, 8, and 12, based on Kanamori, Cabral, and Besser, Besser would not have been combined with the references for the same reasons discussed above. Further, Besser fails to make up for the deficiencies of Kanamori and Cabral discussed above. Thus, claims 2, 4, 5, 7, 8, and 12 are similarly patentable.

Thus, turning to the claim language, there is no teaching or suggestion of "*[a] method for fabricating a silicide for a semiconductor device, said method comprising:*

depositing a metal containing silicon or a metal alloy on a silicon substrate;

reacting said metal containing silicon or said metal alloy to form a first silicide phase;

etching any unreacted metal containing silicon or alloy;

depositing a silicon cap layer over said first silicide phase;

reacting the silicon cap layer to form a second silicide phase, for said semiconductor device; and

etching any unreacted silicon from said silicon cap layer " (emphasis Applicant's), as defined by independent claim 1, and somewhat similarly (but having different and/or additional limitations) in independent claims 4, 10, 13, and 26.

For the reasons stated above, the claimed invention is fully patentable over the cited references.

Further, the other prior art of record has been reviewed, but it too even in combination

with Besser et al., Kanamori, and/or Akram fails to teach or suggest the claimed invention.

IV. FORMAL MATTERS AND CONCLUSION

Applicant appreciates the Examiner's approval of the drawing corrections filed on May 14, 2002. Submitted herewith are corrected formal drawings.

In view of the foregoing, Applicant submits that claims 1-14 and 23-38, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: 1/2/03

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VERSION SHOWING MARKINGS MADE

IN THE CLAIMS:

1. (Amended) A method for fabricating a silicide for a semiconductor device, said method comprising:

depositing a metal containing silicon or [an] a metal alloy [thereof] on a silicon substrate;

reacting said metal containing silicon or said alloy to form a first silicide phase;

etching any unreacted metal containing silicon or alloy;

depositing a silicon cap layer over said first silicide phase;

reacting the silicon cap layer to form a second silicide phase, for said semiconductor device; and

etching any unreacted silicon from said silicon cap layer.

4. (Amended) A method for fabricating a silicide for a silicon region, said method comprising:

depositing a metal containing silicon or [an] a metal alloy [thereof] on a bulk silicon substrate;

reacting said metal containing silicon or said alloy to form a first silicide phase;

etching any unreacted metal containing silicon or alloy;

depositing a silicon cap layer over said first silicide phase;

reacting the silicon cap layer to form a second silicide phase; and

etching any unreacted silicon from said silicon cap layer.

10. (Amended) A method for fabricating a silicide for a silicon region, said method comprising:

depositing a metal or [an] a metal alloy [thereof] on a bulk silicon substrate;

reacting said metal or said alloy to form a first silicide phase;

etching any unreacted metal or alloy;

depositing a silicon cap layer over said first silicide phase;

reacting the silicon cap layer to form a second silicide phase; and

etching any unreacted silicon from said silicon cap layer,

wherein said metal is co-deposited with silicon.

13. (Amended) A method for fabricating a silicide, said method comprising:

providing a substrate having a silicon layer;

depositing a metal containing silicon or [an] a metal alloy over said silicon layer;

reacting said metal containing silicon or said alloy to form a first silicide phase;

etching any unreacted metal containing silicon or alloy; and

depositing a silicon cap layer over said metal containing silicon or said alloy;

reacting the silicon cap layer, to form a second silicide phase; and

etching any unreacted silicon from said silicon cap layer.

25. (Amended) A method for fabricating a silicide for a semiconductor device, said method comprising:

depositing a metal containing silicon or [an] a metal alloy [thereof] on a silicon substrate;

reacting said metal containing silicon or said alloy to form a first forming silicide phase;

etching any unreacted metal or alloy;

depositing a silicon cap layer over said first forming silicide phase;

reacting the silicon cap layer to form a second silicide phase, for said semiconductor device; and

etching any unreacted silicon from said silicon cap layer.

26. (Amended) A method for fabricating a silicide for a silicon region, said method comprising:

depositing a metal containing silicon or [an] a metal alloy [thereof] on a bulk silicon substrate;

reacting said metal containing silicon or said alloy to form a first silicide phase;

etching any unreacted metal containing silicon or alloy;

depositing a silicon cap layer over said first silicide phase;

reacting the silicon cap layer to form a second phase; and

etching any unreacted silicon from said silicon cap layer, wherein said metal is nickel.

Please add the following new claims:

–27. The method of claim 1, wherein said first silicide phase comprises a silicon-rich phase.

28. The method of claim 1, wherein said depositing said metal containing silicon or said alloy thereof containing silicon is for extending a temperature window in which a silicide metal-rich phase exists.

29. The method of claim 4, wherein said first silicide phase comprises a silicon-rich phase.

30. The method of claim 4, wherein said depositing said metal containing silicon or said alloy thereof containing silicon is for extending a temperature window in which a silicide metal-rich phase exists.

31. The method of claim 10, wherein said first silicide phase comprises a silicon-rich phase.

32. The method of claim 10, wherein said depositing said metal containing silicon or said alloy thereof containing silicon is for extending a temperature window in which a silicide metal-rich phase exists.

33. The method of claim 13, wherein said first silicide phase comprises a silicon-rich phase.

34. The method of claim 13, wherein said depositing said metal containing silicon or said alloy thereof containing silicon is for extending a temperature window in which a silicide metal-rich phase exists.

35. The method of claim 25, wherein said first forming silicide phase comprises a silicon-rich

phase.

36. The method of claim 25, wherein said depositing said metal containing silicon or said alloy thereof is for extending a temperature window in which a silicide metal-rich phase exists.

37. The method of claim 26, wherein said first silicide phase comprises a silicon-rich phase.

38. The method of claim 26, wherein said depositing said metal containing silicon or said alloy thereof containing silicon is for extending a temperature window in which a silicide metal-rich phase exists.--